What is claimed is:

1) A circuit, comprising:
   (a) a first node for providing a variable first voltage;
   (b) a second node for providing a variable second voltage;
   (c) a first transistor, coupled to the first node, having a first gate for providing a first current responsive to a first control voltage being applied to the first gate;
   (d) a second transistor, coupled to the second node, having a second gate for providing a second current responsive to a second control voltage being applied to the second gate;
   (e) a first control circuit, coupled to the first gate and the second node, for providing the first control voltage responsive to the variable second voltage; and,
   (f) a second control circuit, coupled to the second gate and the first node, for providing the second control voltage responsive to the variable first voltage.

2) The circuit of claim 1, wherein the first voltage is different from the second voltage.

3) The circuit of claim 1, wherein the first and second transistors operate in a saturation region.

4) The circuit of claim 1, wherein the circuit further comprises:
   (g) a third transistor, coupled to the first node, having a third gate coupled to the first node, for providing a third current responsive to the first variable voltage; and,
   (h) a fourth transistor, coupled to the second node, having a having a fourth gate coupled to the second node, for

providing a fourth current responsive to the second variable voltage.

5) The circuit of claim 4, wherein the first current approximately equals the fourth current and the third current approximately equals the second current.

6) The circuit of claim 1, wherein the first variable voltage and the second variable voltages are obtained from a clock signal.

7) The circuit of claim 6, wherein the clock signal has an amplitude of greater than approximately 400 mv.

8) The circuit of claim 4, wherein the first current, the second current, the third current and the fourth current are used to provide a duty cycle correction signal.

9) The circuit of claim 4, wherein the first transistor, the second transistor, the third transistor and the fourth transistor are n-type transistors.

10) The circuit of claim 4, wherein the first control circuit comprises:

(i) a voltage source;

(j) a fifth transistor, coupled to the voltage source, having a gate;

(k) a sixth transistor, coupled to the fifth transistor, having a gate coupled to the first transistor gate;

(l) a sixth transistor, coupled to the voltage source, having a gate; and,

(m) a seventh transistor, coupled to the sixth transistor, having a gate coupled to the second node.

11) The circuit of claim 10, wherein the second control circuit comprises:

(n) an eighth transistor coupled to the voltage source;

(o) a ninth transistor, coupled to the eighth transistor, having a gate coupled to the first node;

(p) a tenth transistor coupled to the voltage source; and,

(q) an eleventh transistor coupled to the tenth transistor, having a gate coupled to the second transistor gate.

12) The circuit of claim 1, wherein the circuit is a cross-coupled load with a built-in current mirrors circuit used in a double data rate receiving circuit for improving a clock signal.

13) The circuit of claim 1, wherein the circuit is in a memory device.

14) The circuit of claim 1, wherein the circuit is in a memory device controller.

15) A circuit for correcting a duty cycle of a clock signal, comprising:

(a) a first node for providing a variable first voltage representing the clock signal;

(b) a second node for providing a variable second voltage representing the clock signal;

(c) a first transistor, coupled to the first node, having a first gate for providing a first current responsive to a first control voltage being applied to the first gate, wherein the first transistor is operating in a saturation region;

(d) a second transistor, coupled to the second node, having a second gate for providing a second current responsive to a second control voltage being applied to the second gate, wherein the second transistor is operating in a saturation region;

(e) a first control circuit, coupled to the first gate and the second node, for providing the first control voltage responsive to the variable second voltage; and,

(f) a second control circuit, coupled to the second gate and the first node, for providing the second control voltage responsive to the variable first voltage, wherein the first voltage is greater than the second voltage.

16) The circuit of claim 15, wherein the circuit further comprises:

(g) a third transistor, coupled to the first node, having a third gate coupled to the first node, for providing a third current responsive to the first variable voltage; and,

(h) a fourth transistor, coupled to the second node, having a fourth gate coupled to the second node, for providing a fourth current responsive to the second variable voltage.

17) The circuit of claim 16, wherein the first current approximately equals the fourth current and the third current approximately equals the second current.

18) The circuit of claim 17, wherein the first current, the second current, the third current and the fourth current are used to provide a duty cycle correction signal.

19) The circuit of claim 16, wherein the first control circuit comprises:

(i) a voltage source;

(j) a fifth transistor, coupled to the voltage source, having a gate;

(k) a sixth transistor, coupled to the fifth transistor, having a gate coupled to the first transistor gate;

(l) a sixth transistor, coupled to the voltage source, having a gate; and,

(m) a seventh transistor, coupled to the sixth transistor, having a gate coupled to the second node.

20) The circuit of claim 19, wherein the second control circuit comprises:

(n) an eighth transistor coupled to the voltage source;

(o) a ninth transistor, coupled to the eighth transistor, having a gate coupled to the first node;

(p) a tenth transistor coupled to the voltage source; and,

(q) an eleventh transistor coupled to the tenth transistor, having a gate coupled to the second transistor gate.

21) An apparatus, comprising:

(a) a transmit circuit for transmitting serial data; and,

(b) a receive circuit, coupled to the transmit circuit, for generating an output signal responsive to the serial data, wherein the receive circuit includes:

(i) a first node for providing a variable first voltage;

(ii) a second node for providing a variable second voltage;

(iii) a first transistor, coupled to the first node, having a first gate for providing a first current responsive to a first control voltage being applied to the first gate;

(iv) a second transistor, coupled to the second node, having a second gate for providing a second current responsive to a second control voltage being applied to the second gate;

(v) a first control circuit, coupled to the first gate and the second node, for providing the first control voltage responsive to the variable second voltage; and,

(vi) a second control circuit, coupled to the second gate and the first node, for providing the second control voltage responsive to the variable first voltage.

22) The circuit of claim 21, wherein the receiving circuit further comprises:

(vii) a third transistor, coupled to the first node, having a third gate coupled to the first node, for providing a third current responsive to the first variable voltage; and,

(viii) a fourth transistor, coupled to the second node, having a having a fourth gate coupled to the second node, for providing a fourth current responsive to the second variable voltage.

23) The circuit of claim 22, wherein the first current approximately equals the fourth current and the third current approximately equals the second current.

24) The circuit of claim 22, wherein the first control circuit comprises:

(ix) a voltage source;

(x) a fifth transistor, coupled to the voltage source, having a gate;

(xi) a sixth transistor, coupled to the fifth transistor, having a gate coupled to the first transistor gate;

(xii) a sixth transistor, coupled to the voltage source, having a gate; and,

(xiii) a seventh transistor, coupled to the sixth transistor, having a gate coupled to the second node.

25) The circuit of claim 24, wherein the second control circuit comprises:

(xiv) an eighth transistor coupled to the voltage source;

(xv) a ninth transistor, coupled to the eighth transistor, having a gate coupled to the first node;

transistor;

(xvi) a tenth transistor coupled to the voltage source ;and,

(xvii) an eleventh transistor coupled to the tenth transistor, having a gate coupled to the second transistor gate.

26) The apparatus of claim 21, wherein the transmit circuit is included in a memory controller and the receive circuit is included in a memory device.

27) The apparatus of claim 21, wherein the receive circuit is a circuit used for improving a clock signal.

28) A method, comprising the steps of:

(a) obtaining a clock signal;

(b) applying a first voltage from the clock signal to a first transistor operating in a saturation region;

(c) applying a second voltage from the clock signal to a second transistor operating in a saturation region;

(d) providing a first current responsive to applying the first voltage to the first transistor; and,

(e) providing a second current responsive to applying the second voltage to the second transistor.

29) The method of claim 28, further comprising the steps of:

(f) applying the first voltage to a third transistor operating in a saturation region;

(g) applying the second voltage to a fourth transistor operationg in a saturation region;

(h) providing a third current responsive to applying the first voltage to the third transistor;

(i) providing a fourth current responsive to applying the second voltage to the fourth transistor.

30) The method of claim 29, wherein the first current approximately equals the fourth current and the third current approximately equals the second current.

31) The method of claim 28, wherein the first current, the second current, the third current and fourth current are used to provide a duty cycle correction signal.

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